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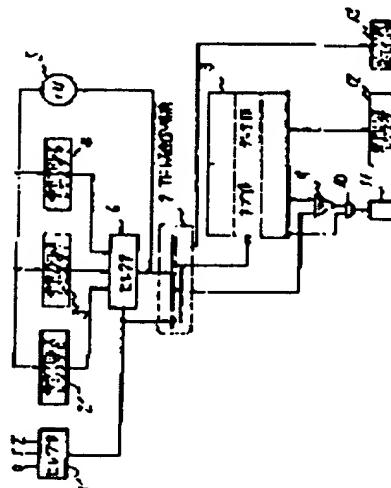
(21)Application number : 03-106252 (71)Applicant : NEC CORP
 (22)Date of filing : 13.05.1991 (72)Inventor : SAKAI NORIAKI

(54) INFORMATION PROCESSOR

(57)Abstract:

PURPOSE: To eliminate the conflict between instruction prefetch addresses of different streams, and to efficiently use the high speed address converting mechanism of a direct map system by synthesizing an address by the selected stream number and a part determined in advance of the instruction prefetch address and setting it as a read/write address, and setting the part determined in advance as a comparison address.

CONSTITUTION: In the information processor provided with an instruction prefetch mechanism for prefetching a multi-stream instruction by using plural instruction buffers and a high speed address converting mechanism of a direct map system, the stream number given in advance to each instruction stream is selected by a selector 6, and an instruction prefetch address related to this instruction stream is selected. An address is synthesized by the selected stream number and a part determined in advance of the instruction prefetch address, its output is set as a read/write address, the part determined in advance is set as a comparison address and index and registration are executed.



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